

where a capping layer consisting of the silicon oxide film according to the invention existed, the sizes of the ridges were less than about 200 Å. Generation of the ridges can be suppressed by subjecting the crystalline silicon film to laser annealing while it is capped with the first dielectric film.--

In the Claims:

Please amend the claims as follows.

Sub D27
C2

2. (Amended) A semiconductor device comprising:
a crystalline semiconductor island comprising silicon over a substrate, said semiconductor island comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and
a gate insulating film comprising a silicon oxide layer and a silicon nitride layer with said silicon nitride layer provided over said silicon oxide layer,
wherein said silicon oxide layer is provided over said crystalline semiconductor island and has a side aligned with a side of said crystalline semiconductor island, and
wherein said crystalline semiconductor island has a ridge on a surface of said semiconductor island, and

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wherein said ridge is less than 500 Å over said channel formation region.

3.(Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon over a substrate, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

an insulating layer comprising a thermal oxide of said semiconductor layer, said thermal oxide being provided in contact with a surface of said semiconductor layer and constituting a part of a gate insulating layer of said semiconductor device; and

a gate electrode provided adjacent to said channel formation region with said gate insulating layer therebetween,

wherein said crystalline semiconductor layer has a ridge on said surface of said semiconductor layer, and

wherein said ridge is less than 500 Å over said channel formation region.

4.(Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon over a substrate, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between

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D2
said source region and said drain region with at least one
lightly doped region between said channel formation region and
at least one of said source region and said drain region;

C2
an insulating layer comprising a thermal oxide of said
semiconductor layer, said thermal oxide being provided in
contact with a surface of said semiconductor layer and
constituting a part of a gate insulating layer of said
semiconductor device; and

a gate electrode provided adjacent to said channel
formation region with said gate insulating layer therebetween,

wherein said crystalline semiconductor layer has a ridge on
said surface of said semiconductor layer, and

wherein said ridge is less than 500 Å over said channel
formation region.

5. (Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon on an
insulating surface, said semiconductor layer comprising a source
region, a drain region, and a channel formation region provided
between said source region and said drain region;

wherein said crystalline semiconductor layer has a ridge on
a surface of said crystalline semiconductor layer, and

wherein said ridge is less than 500 Å over said channel
formation region.

Sub D67
C3
11. (Amended) A semiconductor device comprising:
a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and
an insulating layer comprising silicon oxide or silicon nitride provided on said crystalline semiconductor layer, said insulating layer constituting a part of a gate insulating layer of said semiconductor device,
wherein said crystalline semiconductor layer has a ridge on a surface of said crystalline semiconductor layer, and
wherein said ridge is less than 500 Å over said channel formation region.

Sub D67
16. (Amended) The device of claim 11 wherein the silicon oxide of said insulating layer is formed by wet oxidation or hydrogen chloride oxidation.

Sub D87
18. (Amended) A semiconductor device comprising:
a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region,

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wherein said crystalline semiconductor layer has a ridge measured by AFM on a surface of said crystalline semiconductor layer, and

wherein said ridge is less than 500 Å over said channel formation region.

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D107
24. (Amended) A semiconductor device comprising:
a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

an insulating layer comprising silicon oxide or silicon nitride provided on said crystalline semiconductor layer, said insulating layer constituting a part of a gate insulating layer of said semiconductor device,

wherein said crystalline semiconductor layer has a ridge measured by AFM on a surface of said crystalline layer, and

wherein said ridge is less than 500 Å over said channel formation region.

C1
31. (Amended) A semiconductor device comprising:
a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source

region, a drain region, and a channel formation region provided between said source region and said drain region; and

an insulating layer comprising silicon nitride provided on said crystalline semiconductor layer, said insulating layer constituting a part of a gate insulating layer of said semiconductor device,

wherein said crystalline semiconductor layer has a ridge on a surface of said crystalline semiconductor layer,

wherein said ridge is less than 500 Å over said channel formation region, and

wherein said semiconductor layer is irradiated with a laser light while said insulating layer comprising silicon nitride is provided on said semiconductor layer, in order to suppress formation of said ridge.

35. (Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

an insulating layer comprising silicon oxide provided on said crystalline semiconductor layer, said insulating layer constituting a part of a gate insulating layer of said semiconductor device,

wherein said crystalline semiconductor layer has a ridge on a surface of said crystalline semiconductor layer,

wherein said ridge is less than 500 Å over said channel formation region, and

wherein said semiconductor layer is irradiated with a laser light while said insulating layer comprising silicon oxide is provided on said semiconductor layer, in order to suppress formation of said ridge.

40. (Amended) A semiconductor device comprising:

a crystalline semiconductor layer comprising silicon on an insulating surface, said semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

an insulating layer comprising silicon oxide or silicon nitride provided on said crystalline semiconductor layer, said insulating layer constituting a part of a gate insulating layer of said semiconductor device,

wherein said crystalline semiconductor layer has a ridge measured by AFM on a surface of said crystalline semiconductor layer,

wherein said ridge is less than 500 Å over said channel formation region, and

wherein said semiconductor layer is irradiated with a laser light while said insulating layer is provided on said semiconductor layer in order to suppress formation of said ridge.
